CLAIMS

What is claimed is:

1. A field effect transistor, comprising:

a substrate;

a source and a drain;

an electric field terminal region in the substrate; and

a body above the electric field terminal region between the source and drain, wherein there is a barrier between the electric field terminal region and the body.

2. The transistor of claim 1, wherein the barrier is an insulator layer between the body and the electric field terminal region.

3. The transistor of claim 1, wherein the body is undoped.

4. A field effect transistor, comprising:

an insulator layer;

a body above the insulator layer between a source and a drain;

a substrate below the insulator layer;

a gate above the body and between the source and drain, the gate having a length; and

an electric field terminal region in the substrate.

5. The transistor of claim 4, wherein the body is undoped.

6. The transistor of claim 4, wherein the body is lightly doped.

7. The transistor of claim 4, wherein a channel is formed in the body between the source and drain when certain voltages are applied to the source, gate, and drain, and the channel is undoped.

8. The transistor of claim 4, wherein a threshold voltage is set by a distance between the insulator layer and a gate insulator.

9. The transistor of claim 4, wherein the body floats.

10. The transistor of claim 4, wherein the body is biased.

11. The transistor of claim 4, wherein the electric field terminal region floats.

12. The transistor of claim 4, wherein the electric field terminal region is biased.

13. The transistor of claim 4, wherein the substrate floats.

14. The transistor of claim 4, wherein the substrate is biased.

15. The transistor of claim 4, wherein the electric field terminal region extends beneath essentially the entire length of the gate.

16. The transistor of claim 4, wherein the electric field terminal region extends beneath only a portion of the gate and another electric field terminal region extends beneath another portion of the gate.

17. The transistor of claim 4, wherein the transistor is a pMOSFET.

18. The transistor of claim 4, wherein the transistor is an nMOSFET.

19. The transistor of claim 4, wherein the electric field terminal region extends partially under the source and drain.

20. A die comprising:

first and second field effect transistors each including:

(a) a substrate;

(b) an electric field terminal region in the substrate.

(c) a source and a drain; and

(d) a body above the electric field terminal region between the source and drain.

21. The die of claim 20, further comprising an insulator layer between the substrate and body.

22. The die of claim 20, wherein the insulator layer is shared by the first and second field effect transistor.

23. The die of claim 20, wherein the body is shared by the first and second field effect transistors.

24. The die of claim 20, wherein the electric field terminal region is shared by the first and second field effect transistors.

25. A method of fabricating a field effect transistor, comprising:

implanting an insulator layer into a substrate separating a body from the remainder of the substrate;

implanting an electric field terminating region into the substrate;

forming a source and a drain.

26. The method of claim 25, wherein the insulator layer is implanted before the electric field terminating region is implanted.